

**RTL8711AM**

**SINGLE-CHIP 802.11b/g/n 1T1R WLAN SoC**

**DATASHEET**

#### (CONFIDENTIAL: Development Partners Only)

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##### USING THIS DOCUMENT

This document is intended for the software engineer’s reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

##### REVISION HISTORY

|  |  |  |
| --- | --- | --- |
| **Revision** | **Release Date** | **Summary** |
| 0.0 | 2014/09/30 | Preliminary release. |
| R1V7 | 2015/09/25 | 1. correct feature list 2. modify block diagram 3. correct programming space, IO space and extension memory space 4. correct pin function group table 5. correct memory system 6. modify electrical characteristics |
| R1V8 | 2015/11/10 | 1. modify ADC |
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# General Description

Realtek RTL8711AM is a highly integrated single-chip low power 802.11n Wireless LAN (WLAN) network controller. It combines an ARM-Cortex M3 MCU, WLAN MAC, a 1T1R capable WLAN baseband, and RF in a single chip. It also provides a bunch of configurable GPIOs which are configured as digital peripherals for different applications and control usage.

RTL8711AM integrates internal memories for complete WIFI protocol functions. The embedded memory configuration also provides simple application developments.

# Features

#### General

* Package QFN56
* CMOS MAC, Baseband PHY, and RF in a single chip for 802.11b/g/n compatible WLAN
* Complete 802.11n solution for 2.4GHz band
* 72.2Mbps receive PHY rate and 72.2Mbps transmit PHY rate using 20MHz bandwidth
* 150Mbps receive PHY rate and 150Mbps transmit PHY rate using 40MHz bandwidth
* Compatible with 802.11n specification
* Backward compatible with 802.11b/g devices while operating in 802.11n mode

#### Standards Supported

* 802.11b/g/n compatible WLAN
* 802.11e QoS Enhancement (WMM)
* 802.11i (WPA, WPA2). Open, shared key, and pair-wise key authentication services
* WIFI WPS support
* WIFI Direct support
* Light Weight TCP/IP protocol
* WLAN MAC Features
* Frame aggregation for increased MAC efficiency (A-MSDU, A-MPDU)
* Low latency immediate High-Throughput Block Acknowledgement (HT-BA)
* Long NAV for media reservation with CF-End for NAV release
* PHY-level spoofing to enhance legacy compatibility
* Power saving mechanism

#### WLAN PHY Features

 802.11n OFDM

* One Transmit and one Receive path (1T1R)
* 20MHz and 40MHz bandwidth transmission
* Short Guard Interval (400ns)
* DSSS with DBPSK and DQPSK, CCK modulation with long and short preamble
* OFDM with BPSK, QPSK, 16QAM, and 640QAM modulation. Convolutional Coding Rate: 1/2, 2/3, 3/4, and 5/6
* Maximum data rate 54Mbps in 802.11g and 150Mbps in 802.11n
* Fast receiver Automatic Gain Control (AGC)
* On-chip ADC and DAC

#### Peripheral Interfaces

* 1 high speed UART interface with baud rate up to 4MHz
* 1 log UART with standard baud rate support
* Maximum 3 I2C interface

 I2S with 8/16/24/32/48/96/44.1/88.2 KHz sampling rate

* Maximum 2 PCM with 8/16KHz sample rate
* 1 SPI supported. One supports baud rate up to 20.8 MHz
* Support 4 PWM with configurable duration and duty cycle from 0 ~ 100%
* Support 4 External Timer Trigger Event (ETE function) with configurable period in low power mode
* Support ADC with 1 channel
* Maximum 19 GPIO pins

# Block Diagram

## Functional Block Diagram

3.3V Input

PMU

LP-TIMER POR

Retension SRAM

LP-TIMER

ROM 1MKB

SDRAM 2MB

SoC-ON

CPU

4/10/20/41/

83/166MHz

Flash 0.5~2MB

WIFI

1x1n

Switch Bus

ETE x4

|  |  |
| --- | --- |
| GDMA  12 channel | |
|  |  |
| GTIMER  8 Sets | |

BT

Controller

SPI

Master/Salve

I2S

Master/ Salve

Voice/ Audio Codec

Serial Interface

I2C

I2C

aster/ Salve

I2C

aster/ Salve

Digital Sensor

Master/ Salve

M M

Digital Sensor

2/5/10/20/

HS-UART

41/83MHz

PWM x4

PCM

Master/ Salve e

PCM

Master/ Salv

Voice/ Audio Codec

Controller Config Intf

GPIOs

19 GPIOs

##### Figure 1. Block Diagram

## WIFI and NFC Application Diagram

RTL8711AM

Transmitter

Balun/

Filter Circuit

matching

Receiver

Antenna

NFC Tag Modem/ MCU

TX I/Q

MCU/

Peripheral

Peripheral Interface

. Memory

DAC

PA

Antenna

2.4 GHz

MAC

RX I/Q

ADC

NV Memory

SWR/LDO

Regulators

Baseband ( PHY)

3.3V

40 MHz

Crystal

##### Figure 2. Single-Band 11n (1x1) and NFC Tag Solution

## Power Supply Application Diagram

3.3V

Controllable 1.2V



WLRF

NFC

DCORE

AD/DA

1.8V ~ 2.7

3.3V

PMU

3.3

3.3

V

V

VD33IO

3.3

V

SDRAM

VDDIO

3.

V

1.8V ~ 3.3V

3V

**RTL8711AM**

##### Figure 3. Power Supply Architecture

The integrated Power Management Unit (PMU) provides the following features:

* 1.2V power bulk or LDO selectable.

 1.8~2.7V LDO

* 3.3V power source integrated power cut controlled by FW.

# Memory Mapping

## Programming Space

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Name** | **Mode** | **Physical** | ***Size*** | **IP Function** |
| Code |  | 0x0000\_0000 | 1MB | Instruction Memory (ROM) |
| 0x000F\_FFFF |
| 0x1000\_0000 | 448KB | Inter SRAM: BD SRAM and Buffer SRAM share total 448KB physical  sram |
| 0x1006\_FFFF |
| 0x1FFF\_0000 | 64KB | TCM (Tightly-Coupled Memory) SRAM |
| 0x1FFF\_FFFF |
| SRAM |  | 0x3000\_0000 | 2MB | SDR SDRAM memory |
| 0x301F\_FFFF |

## IO Space

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Name** | **Mode** | **Physical Address** | ***Size*** | **IP Function** |
| Peripheral |  | 0x4000\_0000 | 4KB | SYS Control (SYSON) |
| 0x4000\_0FFF |
| 0x4000\_1000 | 2KB | GPIO Control |
| 0x4000\_17FF |
| 0x4000\_1800 |  | RSVD |
| 0x4000\_1FFF |
| 0x4000\_2000 | 4KB | Timer Control |
| 0x4000\_2FFF |
| 0x4000\_3000 | 1KB | UART for Log |
| 0x4000\_33FF |
| 0x4000\_3400 | 1KB | I2C\_2 Control |
| 0x4000\_37FF |
| 0x4000\_3800 | 1KB | I2C\_3 Control |
| 0x4000\_3BFF |
| 0x4000\_3C00 |  | RSVD |
| 0x4000\_4FFF |
| 0x4000\_5000 | 4KB | SDR SDRAM controller |
| 0x4000\_5FFF |
| 0x4000\_6000 | 4KB | SPI flash controller |
| 0x4000\_6FFF |
| 0x4000\_7000 |  | RSVD |
| 0x4000\_FFFF |
| 0x4001\_0000 | 4KB | ADC |
| 0x4001\_0FFF |
| 0x4001\_1000 | 4KB | DAC |
| 0x4001\_1FFF |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Name** | **Mode** | **Physical** | ***Size*** | **IP Function** |
| Peripheral |  | 0x4004\_0000 | 1KB | UART\_0 Control |
| 0x4004\_03FF |
| 0x4004\_0400 | 1KB | RSVD |
| 0x4004\_07FF |
| 0x4004\_0800 | 1KB | RSVD |
| 0x4004\_0BFF |
| 0x4004\_0C00 |  | RSVD |
| 0x4004\_1FFF |
| 0x4004\_2000 | 1KB | SPI\_0 Control |
| 0x4004\_23FF |
| 0x4004\_2400 | 1KB | RSVD |
| 0x4004\_27FF |
| 0x4004\_2800 | 1KB | RSVD |
| 0x4004\_2BFF |
| 0x4004\_2C00 |  | RSVD |
| 0x4004\_3FFF |
| 0x4004\_4000 | 1KB | RSVD |
| 0x4004\_43FF |
| 0x4004\_4400 | 1KB | I2C\_1 Control |
| 0x4004\_47FF |
| 0x4004\_4800 |  | RSVD |
| 0x4004\_FFFF |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Name** | **Mode** | **Physical** | ***Size*** | **IP Function** |
| Peripheral |  | 0x4005\_0000 | 16KB | RSVD |
| 0x4005\_3FFF |
| 0x4005\_4000 |  | RSVD |
| 0x4005\_7FFF |
| 0x4005\_8000 | 16KB | RSVD |
| 0x4005\_BFFF |
| 0x4005\_C000 |  | RSVD |
| 0x4005\_FFFF |
| 0x4006\_0000 | 2KB | GDMA0 |
| 0x4006\_07FF |
| 0x4006\_0800 | 2KB | RSVD for other DMA |
| 0x4006\_0FFF |
| 0x4006\_1000 | 2KB | GDMA1 |
| 0x4006\_17FF |
| 0x4006\_1800 |  | RSVD for other DMA |
| 0x4006\_1FFF |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Name** | **Mode** | **Physical** | ***Size*** | **IP Function** |
| Peripheral |  | 0x4006\_2000 | 1KB | RSVD |
| 0x4006\_23FF |
| 0x4006\_2400 | 3KB | RSVD |
| 0x4006\_2FFF |
| 0x4006\_3000 | 1KB | I2S\_1 Control |
| 0x4006\_33FF |
| 0x4006\_3400 | 3KB | RSVD |
| 0x4006\_3FFF |
| 0x4006\_4000 | 1KB | PCM\_0 Control |
| 0x4006\_43FF |
| 0x4006\_4400 |  | RSVD |
| 0x4006\_4FFF |
| 0x4006\_5000 | 1KB | PCM\_1 Control |
| 0x4006\_53FF |
| 0x4007\_0000 | 16KB | Security Engine |
| 0x4007\_3FFF |
| 0x4007\_4000 | 48KB | RSVD |
| 0x4007\_FFFF |
| 0x4008\_0000 | 256KB | WIFI REG &  TX/RX FIFO direct map |
| 0x400B\_FFFF |
| 0x400C\_0000 | 256KB | RSVD |
| 0x400F\_FFFF |
| 0x403F\_FFFF | 1MB | RSVD |

## Extension Memory Space

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Name** | **Mode** | **Physical** | ***Size*** | **IP Function** |
| Flash |  | 0x9800\_0000 | 64MB | External flash memory |
| 0x9BFF\_FFFF |

# Pin Assignments

**SW\_LX SW\_GND VDD\_SRC VD33\_IN VD12D VDD\_IO\_M**

**SW\_HV3 VDD\_IO\_M VD12D GPIOA\_6 GPIOA\_7 GPIOA\_5 GPIOA\_3 VD33IO SPI\_M\_DATA1 GPIOF\_5**

**SPI\_M\_CS SPI\_M\_DATA0 SPI\_M\_CLK**

**CHIP\_EN**

**VD12D GPIOC\_3 GPIOC\_2 GPIOC\_1**

**GPIOC\_0 VDD\_IO GPIOC\_4 GPIOC\_5**

**VA33\_SYS ADC\_CH2 CAP\_ADC VA12\_SYS**

**VD12D GPIOE\_0 GPIOE\_1**

**42 41 40 39 38 37 36 35 34 33 32 31 30 29**

**43**

**44**

**45**

**46**

**47**

**48**

**49**

**50**

**28**

**27**

**26**

**25**

**24**

**23**

**22**

**21**

**51**

**52**

**53**

**54**

**55**

**56**

***RTL8711AM***

**LLLLLLL**

**TXXX**

**57 GND (Exposed Pad)**

**20**

**19**

**18**

**17**

**16**

**15**

**1 2 3 4 5 6 7 8 9 10 11 12 13 14**

**GPIOE\_2 GPIOE\_3 GPIOE\_4 VDD\_IO VA12\_RF VA33\_TR RFIO**

##### Figure 4. Pin Assignments

**GPIOB\_0 GPIOB\_1 GPIOB\_2 GPIOB\_3**

**VD33IO VA33\_NFC**

**NFC\_IP NFC\_IN VA12\_AFE**

**XO XI**

**VA33\_SYN\_AFE VA12\_SYN\_PA**

**VA33\_PA**

## Package Identification

“Green” package is indicated by a ‘G’ in the location marked “T” in Figure 2. The version is shown in the location marked ‘VV’, e.g., A0=Version A0

# 

# Pin Descriptions

The following signal type codes are used in the tables:

|  |  |  |  |
| --- | --- | --- | --- |
| I: | Input | O: | Output |
| T/S: | Tri-State bi-directional input/output pin | S/T/S: | Sustained Tri-State |
| O/D: | Open Drain | P: | Power pin |

## Power On Trap Pin

##### Table 1. Power On Trap Pins

|  |  |  |  |
| --- | --- | --- | --- |
| **Symbol** | **Type** | **Pin No** | **Description** |
| NORMAL\_MODE\_SEL | I | 3 | Shared with GPIOB\_2  1: Normal operation mode  0: Enter into test/debug mode |
| BOOT\_SCENARIO | I | 1 | Shared with GPIOB\_0 0: booting from flash  1: booting from internal memory |
| EEPROM\_SEL | I | 33 | Shared with GPIOF\_5  0: Internal NV memory select  1: reserved for internal testing use |
| SD\_DEV\_SEL | I | 38 | Shared with GPIOA\_7 1: SDMMC Host mode  0: SDIO device mode (8711AM not support) |
| ICFG0 | I | 53 | Shared with GPIOC\_0  When NORMAL\_MODE\_SEL is “1”, then ICFG0 is test mode BIT0. |

|  |  |  |  |
| --- | --- | --- | --- |
|  |  |  |  |
| **Symbol** | **Type** | **Pin No** | **Description** |
| ICFG1 | I | 52 | Shared with GPIOC\_1  When NORMAL\_MODE\_SEL is “1”, then ICFG0 is test mode BIT1. |
| ICFG2 | I | 51 | Shared with GPIOC\_2  When NORMAL\_MODE\_SEL is “1”, then ICFG0 is test mode BIT2. |
| ICFG3 | I | 50 | Shared with GPIOC\_3  When NORMAL\_MODE\_SEL is “1”, then ICFG0 is test mode BIT3. |

## Analog to DC Converter

##### Table 2. ADC Pins

|  |  |  |  |
| --- | --- | --- | --- |
| **Symbol** | **Type** | **Pin No** | **Description** |
| ADC\_CH2 | I | 27 | AD converter input |
| CAP\_ADC | P | 26 | Capacitor for AD converter power. |

## RF and NFC

##### Table 3. RF and NFC Pins

|  |  |  |  |
| --- | --- | --- | --- |
| **Symbol** | **Type** | **Pin No** | **Description** |
| NFC\_IP | I | 7 | NFC input differential signal |
| NFC\_IN | I | 8 | NFC input differential signal |
| RF\_IO | IO | 15 | WL RF signal |

***6.4. Power Pins***

##### Table 4. Power Pins

|  |  |  |  |
| --- | --- | --- | --- |
| **Symbol** | **Type** | **Pin No** | **Description** |
| SW\_LX | P | 43 | Switching Regulator Output |
| SW\_HV3 | P | 42 | Switching Regulator Input  Or Linear Regulator input from 3.3V to 1.5V |
| VA33 | P | 6, 12, 14, 16, 28, | 3.3V for Analog Circuit |
| VD33IO | P | 5, 35 | VDD3.3V for Digital IO |
| VDD\_IO | P | 18, 54 | GPIOE and GPIOC group IO power |
| VDD\_IO\_M | P | 41, 48 | Embedded SDR DRAM power |
| VD12D | P | 24, 40, 47, 49 | VDD 1.2V Digital Circuit |
| VA12 | P | 9, 13, 17, 25 | 1.2V for analog blocks |
| SW\_GND | P | 44 | Switching Regulator Ground |

## Clock Pins

##### Table 5. Clock and Other Pins

|  |  |  |  |
| --- | --- | --- | --- |
| **Symbol** | **Type** | **Pin No** | **Description** |
| XI | I | 11 | 40MHz OSC Input  Input of 40MHz Crystal Clock Reference |
| XO | O | 10 | Output of 40MHz Crystal Clock Reference |

## NOR Flash Interface

##### Table 6. NOR Flash Pins

|  |  |  |  |
| --- | --- | --- | --- |
| **Symbol** | **Type** | **Pin No** | **Description** |
| SPI\_M\_CLK | IO | 30 | NOR Flash CLK signal. Multiplexed with GPIOF\_1 . |
| SPI\_M\_DATA0 | IO | 31 | NOR Flash CLK signal. Multiplexed with GPIOF\_2 . |
| SPI\_M\_CS | IO | 32 | NOR Flash CLK signal. Multiplexed with GPIOF\_0 . |
| SPI\_M\_DATA1 | IO | 34 | NOR Flash CLK signal. Multiplexed with GPIOF\_3 . |

## Digital IO Pins

Please refer to section 6 Pin Function Table for more detailed information.

##### Table 7. GPIO Pins

|  |  |  |  |
| --- | --- | --- | --- |
| **Symbol** | **Type** | **Pin No** | **Description** |
| CHIP\_EN | I | 29 | Whole chip enable control. When asserted, chip function is enabled; when de-asserted, whole chip is shutdown. |
| GPIOB\_0 | IO | 1 | GPIO pin. The MUX function can be referred to Pin Function Table. |
| GPIOB\_1 | IO | 2 | GPIO pin. The MUX function can be referred to Pin Function Table. |
| GPIOB\_2 | IO | 3 | GPIO pin. The MUX function can be referred to Pin Function Table. |
| GPIOB\_3 | IO | 4 | GPIO pin. The MUX function can be referred to Pin Function Table. |

|  |  |  |  |
| --- | --- | --- | --- |
| **Symbol** | **Type** | **Pin No** | **Description** |
| GPIOE\_0 | IO | 23 | GPIO pin. The MUX function can be referred to Pin Function Table. |
| GPIOE\_1 | IO | 22 | GPIO pin. The MUX function can be referred to Pin Function Table. |
| GPIOE\_2 | IO | 21 | GPIO pin. The MUX function can be referred to Pin Function Table. |
| GPIOE\_3 | IO | 20 | GPIO pin. The MUX function can be referred to Pin Function Table. |
| GPIOE\_4 | IO | 19 | GPIO pin. The MUX function can be referred to Pin Function Table. |
| GPIOA\_3 | IO | 36 | GPIO pin. The MUX function can be referred to Pin Function Table. |
| GPIOA\_5 | IO | 37 | GPIO pin. The MUX function can be referred to Pin Function Table. |
| GPIOA\_7 | IO | 38 | GPIO pin. The MUX function can be referred to Pin Function Table. |
| GPIOA\_6 | IO | 39 | GPIO pin. The MUX function can be referred to Pin Function Table. |
| GPIOC\_0 | IO | 53 | GPIO pin. The MUX function can be referred to Pin Function Table. |
| GPIOC\_1 | IO | 52 | GPIO pin. The MUX function can be referred to Pin Function Table. |
| GPIOC\_2 | IO | 51 | GPIO pin. The MUX function can be referred to Pin Function Table. |
|  |  |  |  |

|  |  |  |  |
| --- | --- | --- | --- |
| **Symbol** | **Type** | **Pin No** | **Description** |
| GPIOC\_3 | IO | 50 | GPIO pin. The MUX function can be referred to Pin Function Table. |
| GPIOC\_4 | IO | 55 | GPIO pin. The MUX function can be referred to Pin Function Table. |
| GPIOC\_5 | IO | 56 | GPIO pin. The MUX function can be referred to Pin Function Table. |

# Pin Function Table

## Pin Configurable Function Group Summary Table

##### Table 8. Pin Function Group Table

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| PIN name | JTAG | UART Group | I2C Group | SPI Group | I2S Group | PCM Group | WL\_LED | PWM | ETE | WKDT | GPIO INT | Default State | SCHMT |
| GPIOA\_3 |  | UART0\_RTS |  |  |  |  |  |  |  |  |  | PH | O |
| GPIOA\_5 |  | UART0\_CTS |  |  |  |  |  |  |  | D\_STBY0 |  | PH |  |
| GPIOA\_6 |  | UART0\_IN |  |  |  |  |  |  |  |  |  | PH |  |
| GPIOA\_7 |  | UART0\_OUT |  |  |  |  |  |  |  |  |  | HI |  |
| GPIOB\_0 |  | UART\_LOG\_OUT | |  |  |  |  |  | ETE0 |  |  | HI |  |
| GPIOB\_1 |  | UART\_LOG\_IN |  |  |  |  | WL\_LED0 |  | ETE1 | D\_SLP0 |  | PH |  |
| GPIOB\_2 |  |  | I2C3\_SCL |  |  |  |  |  | ETE2 |  |  | HI | O |
| GPIOB\_3 |  |  | I2C3\_SDA |  |  |  |  |  | ETE3 |  | GPIO\_INT | PH |  |
| GPIOC\_0 |  | UART0\_IN |  | SPI0\_CS0 | I2S1\_WS | PCM1\_SYNC | | PWM0 | ETE0 |  |  | HI |  |
| GPIOC\_1 |  | UART0\_CTS |  | SPI0\_CLK | I2S1\_CLK | PCM1\_CLK |  | PWM1 | ETE1 |  | GPIO\_INT | HI | O |
| GPIOC\_2 |  | UART0\_RTS |  | SPI0\_MOSI | I2S1\_SD\_TX | PCM1\_OUT |  | PWM2 | ETE2 |  |  | HI |  |
| GPIOC\_3 |  | UART0\_OUT |  | SPI0\_MISO | I2S1\_MCK | PCM1\_IN |  | PWM3 | ETE3 |  | GPIO\_INT | HI | O |
| GPIOC\_4 |  |  | I2C1\_SDA | SPI0\_CS1 | I2S1\_SD\_RX |  |  |  |  |  | GPIO\_INT | HI |  |
| GPIOC\_5 |  |  | I2C1\_SCL | SPI0\_CS2 |  |  |  |  |  |  | GPIO\_INT | HI | O |
| GPIOE\_0 | JTAG\_TRST | UART0\_OUT | I2C2\_SCL | SPI0\_CS0 |  | PCM0\_SYNC | | PWM0 |  |  |  | PH | O |
| GPIOE\_1 | JTAG\_TDI | UART0\_RTS | I2C2\_SDA | SPI0\_CLK |  | PCM0\_CLK |  | PWM1 |  |  | GPIO\_INT | PH | O |
| GPIOE\_2 | JTAG\_TDO | UART0\_CTS | I2C3\_SCL | SPI0\_MOSI |  | PCM0\_OUT |  | PWM2 |  |  | GPIO\_INT | PH | O |
| GPIOE\_3 | JTAG\_TMS | UART0\_IN | I2C3\_SDA | SPI0\_MISO |  | PCM0\_IN |  | PWM3 |  | D\_STBY3 | GPIO\_INT | PH | O |
| GPIOE\_4 | JTAG\_CLK |  | I2C3\_SCL | SPI0\_CS1 |  |  |  |  |  |  |  | PH | O |

NOTE1: PH = Pull-High, HI = High-impedance

# Functional Description

## Power Management Control Unit

### Features

The PMU provides the following functions: Bulk/LDO to output 1.2V

LDO to output 1.8V ~ 2.5V power source

Integrated power cut to output Vref (input from VD33\_IN) with SW controllable 2 very Low power clock source with less accuracy: 1K and 500K

1 low power 32.768KHz clock source with moderate accuracy Wakeup system detector to resume from low power state

### Power Mode Description

##### Shutdown Mode

CHIP\_EN de-asserts to shutdown whole chip without external power cut components required.

3.3V



IO

Detect

MCU

deassert

PMC TIM

CHIP\_EN

IO Power

##### Deep Sleep Mode

CHIP\_EN keeps high. Enter into Deep Sleep mode by API. The trigger timer period can be configured or GPIOB\_0 can be used as external trigger event. The DLSP trigger timer can be configured with the range 1 ~ 3600 sec.

3.3V



IO

Detect

MCU

Keep High

PMC TIM

CHIP\_EN

TO (Wakeup)

Command

API to Configure

IO (Wakeup)

##### Deep Standby Mode

CHIP\_EN keeps high. Entering into Deep Sleep mode by API. The trigger timer period can be configured or all GPIO group can be used as external trigger event.

3.3V



IO

Detect

MCU

Keep High

PMC TIM

CHIP\_EN

Command

IO

## Memory System

### Memory Architecture

RTL8711AM integrates ROM, internal SRAM, extended SDR DRAM, extended NOR flash to provide applications with a variety of memory requirements.

### Internal ROM

RTL8711AM integrates a 1MB high access-speed and low leakage internal ROM. The internal ROM memory is clocked at a speed up to 166MHz. The ROM lib provides the following functions:

* Boot Code and MCU initialization
* Default UART driver
* Non-flash booting functions and drivers
* Peripheral libraries
* Security function libraries

### Internal SRAM

448KB SRAM is integrated to provide for instruction, data, and buffer usage. The maximum clock speed is up to 166MHz.

An additional 64KB fast access data memory (TCM) is provided for FW data section. The range is 0x1FFF-0000 ~ 0x1FFF-FFFF.

### Extended SDR DRAM

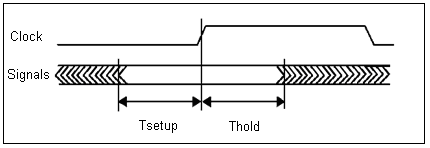
##### Features

* Interface (Bus Width): 16-bit
* Targeted SDR Frequency: Up to 83MHz
* Supports one Chip Select (MCS0#) and 1 Band select (BA0)

##### SDR DRAM Input Timing

##### Table 9. SDR DRAM Input Timing

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Min.** | **Typ.** | **Max.** | **Units** |
| TSETUP | Input Setup Prior to Rising Edge of Clock  Inputs included in this timing are MD[15:0] (during a read operation) | - | 1.13 | - | ns |
| THOLD | Input Hold Time after the Rising Edge of Clock  Inputs included in this timing are MD[15:0] (during a read operation) | - | 0 | - | ns |
| Note: The RTL8196EU integrates some timing controls on the interface. Here the timing parameters listed in the table are extracted in the default situation (without specific controls). | | | | | |

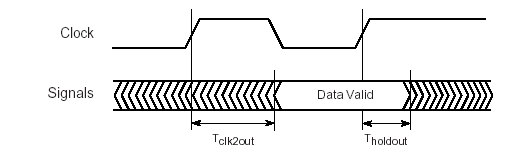


##### Figure 5. SDR DRAM Input Timing

* + - 1. **SDR DRAM Output Timing**

##### Table 10. SDR DRAM Output Timing

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Min.** | **Typ.** | **Max.** | **Units** |
| TCLK2O UT | Rising Edge of Clock-to-Signal Output  Outputs include this timing are MD[15:0], MCS0#, MCS1#, RAS#, CAS#, LDQM, UDQM, WE# (during a write operation) | - | - | 2.3 | ns |
| THOLDO UT | Signal Output Hold Time after the Rising Edge of the Clock  Outputs included in this timing are MD[15:0] (during a write operation) | 0.8 | - | - | ns |
| *Note: Timing was tested with 75-pF capacitor to ground.* | | | | | |

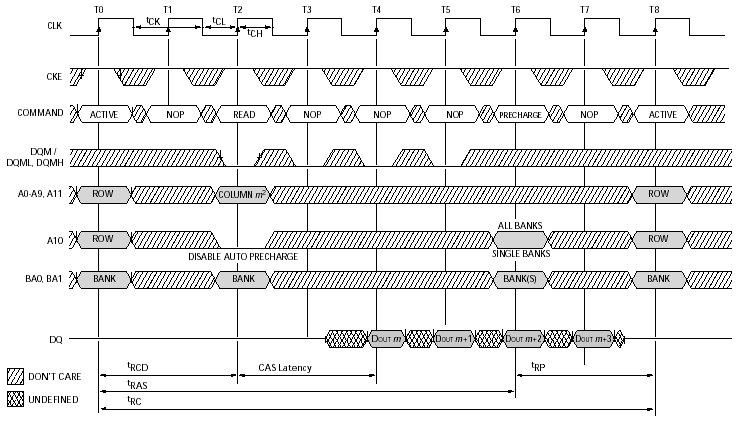


##### Figure 6. SDR DRAM Output Timing

* + - 1. **SDR DRAM Access Control Timing**

##### Table 11. SDR DRAM Access Control Timing

|  |  |  |  |
| --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Units** | **Notes** |
| TREFRESH | Auto-Refresh Timing  Controlled by Reg. 0xB8001008 (DTR) | µs | - |
| TRCD | The Time Interval between RAS# Active and CAS# Active  Controlled by Reg. 0xB8001008 (DTR) | ns | - |
| TRP | The Time Interval between Pre-Charge and the Next Active  Controlled by Reg. 0xB8001008 (DTR) | ns | - |
| TRAS | The Time Interval between Active and Pre-Charge  Controlled by Reg. 0xB8001008 (DTR) | ns | - |
| TRC | The Time Interval between Active and the Next Active  Controlled by Reg. 0xB8001008 (DTR) | ns | 1 |
| TRFC | The Time Interval between Auto-Refresh and Active  Controlled by Reg. 0xB8001008 (DTR) | ns | - |
| TCAS\_LATE NCY | The Data Output Delay after CAS# Active  Controlled by Reg. 0xB8001004 (DCR) | ns | - |
| Note 1: TRC=TRAS+TRP. | | | |



##### Figure 7. SDR DRAM Access Control Timing

### SPI NOR Flash

##### Features

* Targeted SPI flash frequency: Up to 83.3MHz (when CPU clock is 166MHz)
* In addition to a programmed I/O interface, also supports a memory-mapped I/O interface for read operation
* Supports Read and Fast Read in memory-mapped I/O mode

##### Supported NOR Flash List

**Table 12. Flash Bus DC Parameters**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Vendor** | **Part Number** | **Density** | **Voltage** | **IO** |
| MXIC | MXIC\_MX25L4006E | 4M Bits | 3.3V | 1I/2O |
| MXIC | MXIC\_MX25L8073E | 8M Bits | 3.3V | 1I/2O |
|  |  |  |  |  |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Vendor** | **Part Number** | **Density** | **Voltage** | **IO** |
| MXIC | MXIC\_MX25L8006E | 8M Bits | 3.3V | 1I/2O |

##### Electrical Specifications

##### Table 13. Flash Bus DC Parameters

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Conditions** | **Min.** | **Typ.** | **Max.** | **Units** | **Notes** |
| VIH | Input-High Voltage | LVTTL | 2.0 | - | - | V | 1 |
| VIL | Input-Low Voltage | LVTTL | - | - | 0.8 | V | 2 |
| VOH | Output-High Voltage | - | 2.4 | - | - | V | 3 |
| VOL | Output-Low Voltage | - | - | - | 0.4 | V | 3 |
| IIL | Input-Leakage Current | VIN=3.3V or 0 | -10 | 1 | 10 | A | - |
| IOZ | Tri-State Output-Leakage Current | - | -10 | 1 | 10 | A | - |
| RPU | Input Pull-Up Resistance | - | - | 75 | - | KΩ | 4 |
| RPD | Input Pull-Down Resistance | - | - | 75 | - | KΩ | 4 |
| *Note 1: VIH overshoot: VIH (MAX)=VDDH + 2V for a pulse width 3ns.*  *Note 2: VIL undershoot: VIL (MIN)=-2V for a pulse width 3ns.*  *Note 3: The output current buffer is 8mA for the flash address and data bus; and is 8mA for Flash control signals. Note 4: These values are typical values checked in the manufacturing process and are not tested.* | | | | | | | |

## General Purpose DMA Controller

### Features of GDMA

* Dual port DMA with totally 12 channels
* Configurable endian
* Support memory-memory, memory-peripheral, peripheral-memory, and peripheral-peripheral DMA transfer
* Support block level flow control
* Support address auto-reload, link-listed mode
* Support scatter-gather mode

## General Purpose Timer (GTimer)

### Features of GTIMER

* 8 Gtimer supported
* Source clock is 32.768KHz
* Support Counter mode and timer mode

## GPIO Functions

### Features of GPIO

* GPO and GPI function
* Support interrupt detection with configurable polarity per GPIO
* Internal weak pull up and pull low per GPIO
* Multiplexed with other specific digital functions

## UART Interface Characteristics

### Features of UART

* Support 1 HS-UARTs (max baud rate 4MHz and DMA mode) or 1 low speed UARTs (IO mode)
* UART (RS232 Standard) Serial Data Format
* Transmit and Receive Data FIFO
* Programmable Asynchronous Clock Support
* Auto Flow Control
* Programmable Receive Data FIFO Trigger Level
* DMA data moving support to save CPU loading

### High Speed UART Specification

The RTL8711AM UART interface is a standard 4-wire interface with RX, TX, CTS, and RTS. The default baud rate is 115.2k baud. In order to support high and low speed baud rate, the RTL8711AM provides multiple UART clocks.

##### Table 14. UART Baud Rate Specifications

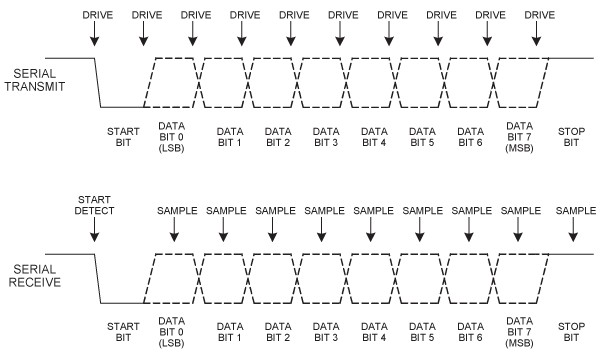
|  |  |  |
| --- | --- | --- |
| **Desired Baud Rate** | **Actual Baud Rate** | **Error (%)** |
| 300 | 300 | 0.00% |
| 600 | 600 | 0.00% |
| 900 | 900 | 0.00% |
| 1200 | 1200 | 0.00% |
| 1800 | 1800 | 0.00% |
| 2400 | 2400 | 0.00% |
| 3600 | 3601 | 0.03% |
| 4800 | 4798 | -0.04% |
| 7200 | 7198 | -0.03% |
| 9600 | 9603 | 0.03% |
|  |  |  |

|  |  |  |
| --- | --- | --- |
| **Desired Baud Rate** | **Actual Baud Rate** | **Error (%)** |
| 14400 | 14395 | -0.03% |
| 19200 | 19182 | -0.09% |
| 28800 | 28846 | 0.16% |
| 38400 | 38462 | 0.16% |
| 56000 | 55970 | -0.05% |
| 57600 | 57692 | 0.16% |
| 76800 | 76531 | -0.35% |
| 115200 | 115385 | 0.16% |
| 128000 | 127119 | -0.69% |
| 153600 | 153061 | -0.35% |

|  |  |  |
| --- | --- | --- |
| **Desired Baud Rate** | **Actual Baud Rate** | **Error (%)** |
| 2000000 | 2000000 | 0.00% |
| 2100000 | 2083333 | -0.79% |
| 2764800 | 2777778 | 0.47% |
| 3000000 | 3000000 | 0.00% |
| 3250000 | 3250000 | 0.00% |
| 3692300 | 3703704 | 0.31% |
| 3750000 | 3750000 | 0.00% |
| 4000000 | 4000000 | 0.00% |

|  |  |  |
| --- | --- | --- |
|  |  |  |
| **Desired Baud Rate** | **Actual Baud Rate** | **Error (%)** |
| 230400 | 229167 | -0.54% |
| 460800 | 458333 | -0.54% |
| 500000 | 500000 | 0.00% |
| 921600 | 916667 | -0.54% |
| 1000000 | 1000000 | 0.00% |
| 1382400 | 1375000 | -0.54% |
| 1444444 | 1437500 | -0.48% |
| 1500000 | 1500000 | 0.00% |
| 1843200 | 1833333 | -0.54% |

##### Figure 8. UART Interface Waveform



* + 1. **UART Interface Signal Levels**

The UART signal level ranges from 1.8V to 3.3V. The host provides the power source with the targeted power level to the RTL8711AM UART interface via the IO power.

## SPI Interface

### Features of SPI

* Support 1 SPI port
* Support Master/Slave mode
* Support DMA to offload CPU bandwidth
* 1 high speed SPI
  + Support up to 3 CS (multi-slave mode up to 3 slave)
  + Support baud rate up to 20MHz (Master mode)
  + Support baud rate up to 5MHz (Slave mode Rx only)
  + Support baud rate up to 4MHz (Slave mode TRx)
* Programmable clock bit-rate
* Programmable clock polarity and phase
* Multiple Serial Interface Operations support
  + Motorola - SPI
  + Texas Instruments - SSI
  + National Semiconductor - Microwire

## I2C Interface

### Features of I2C

* Support maximum 3 I2C port
* Three speeds:
  + Standard mode (0 to 100 Kb/s)
  + Fast mode (<400 Kb/s)
  + High-speed mode (<3.4 Mb/s) (with appropriate bus loading)
* Master or Slave I2C operation
* 7- or 10-bit addressing
* Transmit and receive buffers
* TX and RX DMA support (I2C-1 only)

## PWM Interface

### Features of PWM

* Support maximum 4 PWM functions
* 0~100% duty can be configurable
* Minimum resolution is 64us
* The period can be configured up to 8 seconds

## External Trigger Event Interface

### Features of External Trigger Event

* Support maximum 4 External Trigger Event functions without CPU active
* Triggered by GTIMER

## I2S Interface Characteristics

### Features of I2S

 Support 8/16/24/32/48/96KHz, 44.1/88.2KHz

* Support 16 or 24 bits format
* Integrated DMA engine to minimize SW efforts
* Support TX and RX direction
* Master or Slave mode support

## PCM Interface Characteristics

### Features of PCM

* The RTL8711AM supports a PCM digital audio interface that is used for transmitting digital audio/voice data to/from the Audio Codec. Features are supported as below:
* Supports Master and Slave mode
* Programmable long/short Frame Sync
* Supports 8-bit A-law/µ-law, and 13/16-bit linear PCM formats
* Supports sign-extension and zero-padding for 8-bit and 13-bit samples
* Supports padding of Audio Gain to 13-bit samples
* PCM Master Clock Output: 64, 128, 256, or 512kHz
* Supports SCO/ESCO link
  1. ***AD Converter***

### Features

* 1 16-bit high resolution A/D converter (ADC\_CH2 only)
  + Bandwidth 48KHz
  + Input signal range: 0.01V ~ VREF - 0.2V
* Support DMA mode
* Support One-Shot sampling mode without CPU active to save power
  + Pre-configured period to auto-sampling
  + Support two wakeup method: buffer threshold interrupt and event trigger

## Security Engine

### Features

* Provide low SW computing and high performance encryption
* Supported authentication algorithms:
  + MD5
  + SHA-1

 SHA-2 (SHA-224 / SHA-256 )

* + HMAC-MD5
  + HMAC-SHA1
  + HMAC-SHA2
* Supported Encryption / Decryption mechanisms:
  + DES ( CBC / ECB )
  + 3DES ( CBC / ECB )
  + AES-128 ( CBC / ECB / CTR )
  + AES-192 ( CBC / ECB / CTR )
  + AES-256 ( CBC / ECB / CTR )

# Electrical Characteristics

## Temperature Limit Ratings

##### Table 15. Temperature Limit Ratings

|  |  |  |  |
| --- | --- | --- | --- |
| **Parameter** | **Minimum** | **Maximum** | **Units** |
| Storage Temperature | -55 | +125 | C |
| Ambient Operating Temperature(CS) | -20 | +85 | C |
| Ambient Operating Temperature(IS)1 | -40 | +105 | C |
| Junction Temperature | 0 | +125 | C |

NOTE1: ONLY RTL8711AM-VT1-CG satisfies the industrial standards (IS).

## Temperature Characteristics

##### Table 16. Thermal Properties

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Power (w)** | **PCB (layer)** | **Theat ja (C/W)** | **Theta jc (C/W)** | **Psi jt (C/W)** |
| 1 | 2 | 31 | 10.1 | 0.27 |
| 1 | 4 | 24.5 | 9.4 | 0.21 |

## Power Supply DC Characteristics

##### Table 17. Power Supply DC Characteristics

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Minimum** | **Typical** | **Maximum** | **Units** |
| VA33, VD33IO, SW\_HV3 | 3.3V Supply Voltage | 3.0 | 3.3 | 3.6 | V |
| VDD\_IO | Digital IO Supply Voltage | 1.62 | 1.8~3.3 | 3.6 | V |
| VA12\_AFE, VA12\_SYN, VA12\_RF | 1.2V Core Supply Voltage | 1.08 | 1.2 | 1.32 | V |
| IDD33 | 3.3V Rating Current (with internal regulator and integrated CMOS PA) | - | - | 450 | mA |
|  |  |  |  |  |  |



|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |
| **Symbol** | **Parameter** | **Minimum** | **Typical** | **Maximum** | **Units** |
| IDD\_IO | IO Rating Current (including VDD\_IO) |  |  | 200 | mA |
| IDD\_IO\_33 | 3.3V IO Rating Current |  |  | 50 | mA |

## Digital IO Pin DC Characteristics

### Electrical Specifications

##### Table 18. Typical Digital IO DC Parameters (3.3V Case)

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Conditions** | **Min.** | **Typ.** | **Max.** | **Units** |
| VIH | Input-High Voltage | LVTTL | 2.0 | - | - | V |
| VIL | Input-Low Voltage | LVTTL | - | - | 0.8 | V |
| VOH | Output-High Voltage | LVTTL | 2.4 | - | - | V |
| VOL | Output-Low Voltage | LVTTL | - | - | 0.4 | V |
| VT+ | Schmitt-trigger High Level |  | 1.78 | 1.87 | 1.97 | V |
| VT- | Schmitt-trigger Low Level |  | 1.36 | 1.45 | 1.56 | V |
| IIL | Input-Leakage Current | VIN=3.3V or 0 | -10 | 1 | 10 | A |

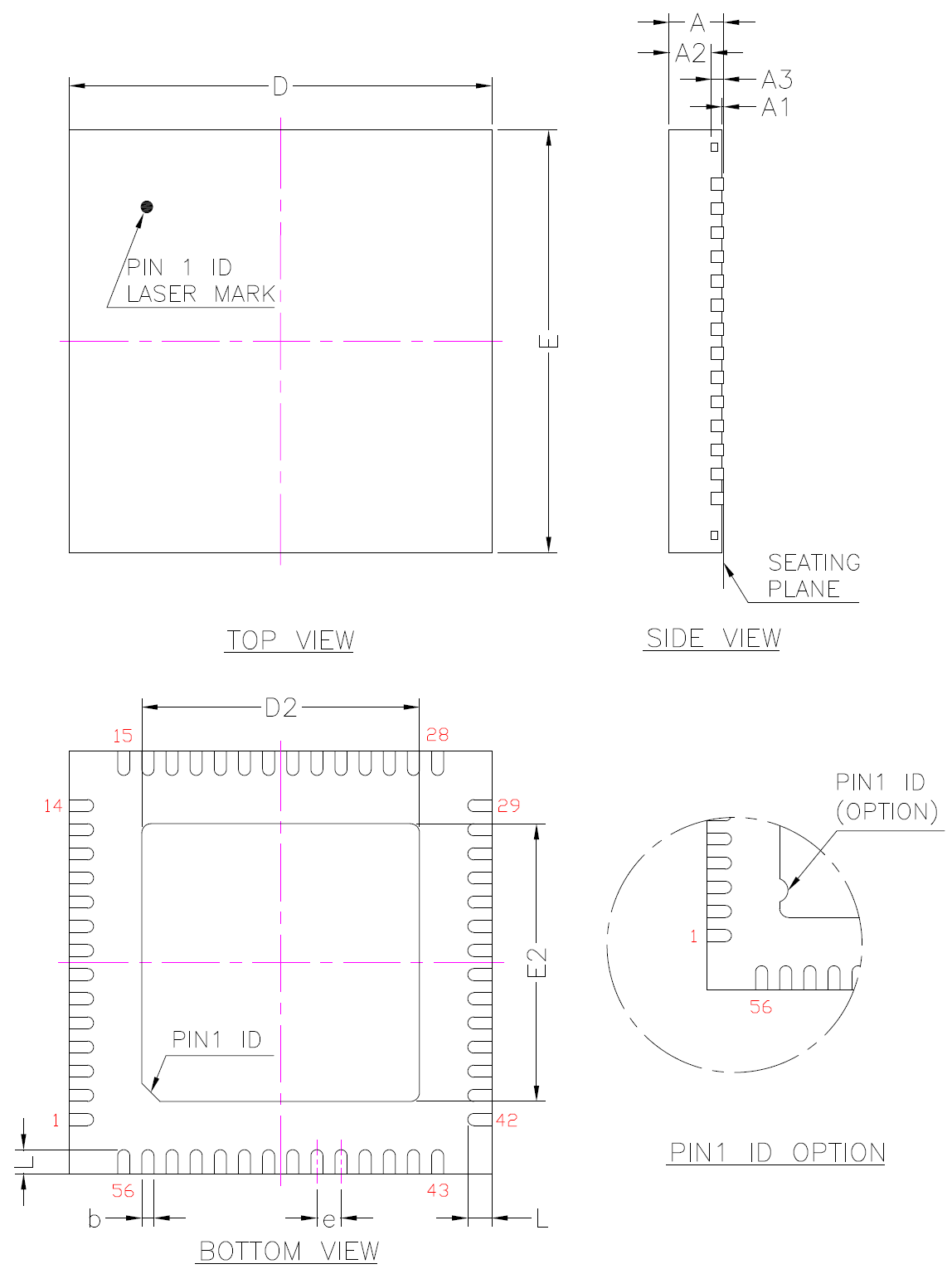
##### Table 19. Typical Digital IO DC Parameters (1.8V Case)

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Conditions** | **Min.** | **Typ.** | **Max.** | **Units** |
| VIH | Input-High Voltage | CMOS | 0.65x VCC | - | - | V |
| VIL | Input-Low Voltage | CMOS | - | - | 0.35x VCC | V |
| VOH | Output-High Voltage | CMOS | VCC-0.45 | - | - | V |
| VOL | Output-Low Voltage | CMOS | - | - | 0.45 | V |
| VT+ | Schmitt-trigger High Level |  | 1.02 | 1.09 | 1.14 | V |
| VT- | Schmitt-trigger Low Level |  | 0.67 | 0.73 | 0.8 | V |
| IIL | Input-Leakage Current | VIN=1.8V or 0 | -10 | 1 | 10 | A |



# Mechanical Dimensions

## Package Specification



## Mechanical Dimensions Notes

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Symbol |  | Dimension in mm |  |  | Dimension in inch |  |
|  | Min | Nom | Max | Min | Nom | Max |
| A | 0.80 | 0.85 | 0.90 | 0.031 | 0.033 | 0.035 |
| A1 | 0.00 | 0.02 | 0.05 | 0.000 | 0.001 | 0.002 |
| A2 | --- | 0.65 | 0.70 | --- | 0.026 | 0.028 |
| A3 |  | 0.2 REF |  |  | 0.008 REF |  |
| b | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 |
| D/E |  | 7.00 BSC |  |  | 0.276 BSC |  |
| D2/E 2 | 4.35 | 4.60 | 4.85 | 0.171 | 0.181 | 0.191 |
| e |  | 0.40 BSC |  |  | 0.016 BSC |  |
| L | 0.30 | 0.40 | 0.50 | 0.012 | 0.016 | 0.020 |

Notes：

1. CONTROLLING DIMENSION：MILLIMETER(mm).
2. REFERENCE DOCUMENTL：JEDEC MO-220.

# Ordering Information

##### Table 20. Ordering Information

|  |  |  |
| --- | --- | --- |
| **Part Number** | **Package** | **Status** |
| RTL8711AM-VA0-CG | QFN-56, ‘Green’ Package | Mass Production |
| RTL8711AM-VB1-CG | QFN-56, ‘Green’ Package | Mass Production |
| RTL8711AM-VT1-CG | QFN-56, ‘Green’ Package | Mass Production |
| *Note: See page 13 for package identification.* | | |

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